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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,178	02/24/2004	Jang-Kun Song	6192.0164.C1	1140

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EXAMINER	
SCHECHTER, ANDREW M	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,178	SONG ET AL.	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26,27,29-32 and 34-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26,27,29-32 and 34-40* is/are rejected.

7)☒ Claim(s) *41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/853,642.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 24 January 2005 has been entered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 35-40 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,788,356

in view of *Yanagisawa,* U.S. Patent No. 5,128,786. Although the conflicting claims are not identical, they are not patentably distinct from each other for the following reasons.

Claim 2 recites all the limitations of claim 35 except that the black matrix is "disconnected at portions thereof" and the buffer layer "covering a gap between the disconnected portions of the black matrix". However, claim 2 recites "the buffer layer being formed between portions of the black matrix". This line seems to imply that there are disconnected portions of the black matrix, and does state that the buffer layer covers a gap between those portions. Assuming for the sake of argument that the portions might be connected in some way, it would have been obvious to one of ordinary skill in the art at the time of the invention to have them disconnected, since *Yanagisawa* teaches having the black matrix disconnected at portions between the two adjoining gate lines, since this reduces display defects which would otherwise be caused by short-circuits between the black matrix and the other electrodes [col. 2, lines 42-49]. Claim 35 would therefore have been obvious to one of ordinary skill in the art at the time of the invention over claim 2.

Claim 2 discloses the gate line formed on the black matrix, the black matrix mesh-shaped ("as a net"), the gate and buffer layer in the same plane, and the method of making such an LCD, so claims 36-40 are also rejected over claim 2.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 35-40 are rejected under 35 U.S.C. 102(e) as being anticipated by *Murade*, U.S. Patent No. 6,297,862.

Murade discloses [see Figs. 1, 2, 5, 6, etc.] a liquid crystal display (LCD) comprising a substrate [10], a black matrix [7] formed on the substrate and disconnected at portions thereof [see Fig. 1]; a gate line [2] formed on the substrate; a data line [3] intersecting the gate line; and a buffer layer [2f] covering a gap between the disconnected portions of the black matrix [see Fig. 1, etc.]. Claim 35 is therefore anticipated.

The gate line is formed on the black matrix [see Fig. 2], so claim 36 is also anticipated. The black matrix is mesh-shaped [see Fig. 1], so claim 37 is also anticipated. The gate line and the buffer layer are formed on the same plane, so claim 38 is also anticipated.

Murade discloses a method of making this LCD, so claim 39 is also anticipated. The method includes forming a conductive layer and patterning it to simultaneously form the gate line and the buffer layer, so claim 40 is also anticipated.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 26, 27, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Han et al.,* U.S. Patent No. 5,926,235 in view of *Yanagisawa,* U.S. Patent No. 5,128,786.

Han discloses [see Fig. 6, for instance] a liquid crystal display comprising a first insulating substrate [110], a gate line assembly [107] with gate lines and gate electrodes [see Fig. 4, 107 and 117], a gate insulating pattern [109], a semiconductor pattern [111], an ohmic contact layer [112], a data line assembly with source and drain electrodes [105 and 106] and data lines [115], and a protective layer [113a] covering the data line and gate line assemblies while exposing the gate insulating pattern, the semiconductor pattern, and the substrate below the gate insulating pattern (where the insulating layer is located in the claimed invention) at the pixel areas [compare Figs 6a and 6b with the application's Fig. 2].

Han does not disclose a black matrix formed on the substrate, mesh-shaped with opening portions exposing pixel areas and disconnected at portions thereof, and an insulating layer on and covering the black matrix and substrate. *Yanagisawa* does disclose a black matrix [16, 26, 36, or 46] formed on an analogous substrate for an analogous device, mesh-shaped with openings exposing the pixel areas and

disconnected at portions thereof, and an insulating layer [17] on and covering the black matrix and substrate. The rest of the structure (electrodes, alignment layer, etc.) is then layered on top of this insulating layer. Note that although the figures in *Yanagisawa* depict a passive matrix LCD with simple lines of electrodes, *Yanagisawa* explicitly says that its invention (the black matrix in discontinuous portions, separated from the electrodes above by an insulating layer) "can also be applied to the liquid crystal display devices of the TFT active matrix type" [col. 8, lines 20-26]. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to form the black matrix and insulating layer of *Yanagisawa* under the gate electrode structure of *Han*, motivated by *Yanagisawa's* teachings that the use of a black matrix prevents light from "leaking through the net-like area ... between the image elements" [col. 1, lines 14-23] so a black matrix is beneficial, and that the use of this particular black matrix (discontinuous, with various portions) reduces display defects which would otherwise be caused by short-circuits between the black matrix and the other electrodes [col. 2, lines 42-49].

Han does not necessarily disclose an alignment film on top of the TFT substrate. *Yanagisawa* does disclose an alignment film [18] on top of its substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to have such an alignment film in the device of *Han*, motivated by the desire to give the proper initial alignment to the liquid crystal molecules and produce a functioning device. This layer would then be a buffer layer covering a gap between disconnected portions of the black matrix [the alignment layer covers the entire substrate, including the gap].

Claim 26 is therefore unpatentable.

Han also discloses a pixel electrode [104] connected to the drain electrode, the contact made through a first contact hole [116] in the protective layer. Claim 27 is therefore also unpatentable. *Yanagisawa*'s black matrix comprises (when combined with *Han*) first portions overlapped with the gate lines, and second portions overlapped with the data lines [see Fig. 7, particularly, though Figs. 6, 8, and 9 also show this]. Claim 29 is therefore also unpatentable.

8. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Han et al.*, U.S Patent No. 5,926,235 in view of *Yanagisawa*, U.S. Patent No. 5,128,786 as applied to claims 26, 27, and 29 above, and further in view of *Murade,* U.S. Patent No. 6,297,862.

The additional limitation is that the pixel electrode has a peripheral portion overlapping the black matrix. *Han* does not disclose a black matrix. *Yanagisawa* discloses a black matrix [see Figs. 6-9] which overlaps its transparent display electrodes (where the pixel electrode would be in an active matrix device), but does not explicitly disclose a pixel electrode or give a teaching explaining why it is beneficial to have the black matrix and the transparent display electrodes overlap as they are depicted doing.

Murade discloses an active matrix LCD with a pixel electrode [14] and a black matrix [7] on the substrate, separated from the other electrodes by an insulating layer [11], analogous to both *Yanagisawa* and the present invention. (The black matrix in *Murade* is also divided into portions.) *Murade* discloses that the black matrix overlaps the pixel electrode [col. 14, lines 66-67] and teaches that this arrangement dispenses

with the need for precise alignment of a black matrix on the opposite substrate, and that the thus obtained liquid crystal devices show little variation in light transmittance [col. 14, line 47 – col. 15, line 17]. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to overlap the pixel electrode and the black matrix, motivated by the example and teaching of *Murade*. Claim 30 is therefore unpatentable.

9. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Han et al.,* U.S. Patent No. 5,926,235 in view of *Yanagisawa,* U.S. Patent No. 5,128,786, and further in view of *Ishiguro*, U.S. Patent No. 5,956,103.

Han discloses [see Fig. 6, for instance] a method for fabricating a TFT substrate for a liquid crystal display comprising having a first insulating substrate [110], forming a gate line assembly [107] with gate lines and gate electrodes [see Fig. 4, 107 and 117], depositing a gate insulating pattern [109], a semiconductor pattern [111], forming an ohmic contact layer [112], a data line assembly with source and drain electrodes [105 and 106] and data lines [115], depositing a protective layer [113a] covering the data line and gate line assemblies, and forming opening portions exposing the substrate (where the insulating layer is located in the claimed invention) through patterning the protective layer, the gate insulating pattern, and the semiconductor pattern [compare Figs 6a and 6b with the application's Fig. 2].

Han does not disclose a black matrix formed on the substrate, mesh-shaped with opening portions exposing pixel areas and disconnected at portions thereof, and an insulating layer on and covering the black matrix and substrate. *Yanagisawa* does

disclose a black matrix [16] formed on an analogous substrate for an analogous device, mesh-shaped with openings exposing the pixel areas and disconnected at portions thereof, and an insulating layer [17] on and covering the black matrix and substrate. The rest of the structure (electrodes, alignment layer, etc.) is then layered on top of the insulating layer. Note that although the figures in *Yanagisawa* depict a passive matrix LCD with simple lines of electrodes, *Yanagisawa* explicitly says that its invention (the black matrix in discontinuous portions, separated from the electrodes above by an insulating layer) "can also be applied to the liquid crystal display devices of the TFT active matrix type" [col. 8, lines 20-26]. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to form the black matrix and insulating layer of *Yanagisawa* under the gate electrode structure of *Han*, motivated by *Yanagisawa's* teachings that the use of a black matrix prevents light from "leaking through the net-like area ... between the image elements" [col. 1, lines 14-23] so a black matrix is beneficial, and that the use of this particular black matrix (discontinuous, with various portions) reduces display defects which would otherwise be caused by short-circuits between the black matrix and the other electrodes [col. 2, lines 42-49].

Han does not necessarily disclose an alignment film on top of the TFT substrate. *Yanagisawa* does disclose an alignment film [18] on top of its substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to have such an alignment film in the device of *Han*, motivated by the desire to give the proper initial alignment to the liquid crystal molecules and produce a functioning device. This layer

would then be a buffer layer covering a gap between disconnected portions of the black matrix [the alignment layer covers the entire substrate, including the gap].

Han also does not disclose that the gate lines and data lines are narrower than the black matrix. This is not taught by either *Han* or *Yanagisawa*, since it compares two features, one from each reference. However, *Ishiguro* teaches that "a black matrix is provided to prevent light from leaking from the periphery of each pixel electrode ... [and] is typically formed with margins to ensure that no light leaks from the periphery of each pixel electrode" [col. 1, lines 31-35]. (Also note again *Yanagisawa's* teaching above regarding the use of a black matrix to prevent light leaking through "between image elements", in this case the pixel electrodes.) Thus, a purpose of the black matrix is to cover the gaps between the display electrodes in a passive matrix display (as shown in *Yanagisawa*), or the gaps between the pixel electrodes in an active matrix display (as in *Han*), to prevent light leakage and improve the display quality. As can be seen in *Han,* the width of the gate and data lines is less than the gaps between the pixel electrodes which are to be covered by the black matrix. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to have the black matrix wider than the gate lines and the date lines, motivated by the desire to have the black matrix cover the pixel electrode periphery and ensure that no light leaks through, as taught by *Ishiguro*.

Claim 31 is therefore unpatentable.

Han also discloses forming a pixel electrode [104] connected to the drain electrode, the contact made through a first contact hole [116] in the protective layer. Claim 32 is therefore also unpatentable.

10. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Han et al.,* U.S. Patent No. 5,926,235,*Yanagisawa,* U.S. Patent No. 5,128,786, and *Ishiguro*, U.S. Patent No. 5,956,103 as applied to claims 31 and 32 above, and further in view of *Murade,* U.S. Patent No. 6,297,862.

The additional limitation is that the pixel electrode has a peripheral portion overlapping the black matrix. *Han* does not disclose a black matrix. *Yanagisawa* discloses a black matrix [see Figs. 6-9] which overlaps its transparent display electrodes (where the pixel electrode would be in an active matrix device), but does not explicitly disclose a pixel electrode or give a teaching explaining why it is beneficial to have the black matrix and the transparent display electrodes overlap as they are depicted doing.

Murade discloses an active matrix LCD with a pixel electrode [14] and a black matrix [7] on the substrate, separated from the other electrodes by an insulating layer [11], analogous to both *Yanagisawa* and the present invention. (The black matrix in *Murade* is also divided into portions.) *Murade* discloses that the black matrix overlaps the pixel electrode [col. 14, lines 66-67] and teaches that this arrangement dispenses with the need for precise alignment of a black matrix on the opposite substrate, and the thus obtained liquid crystal devices show little variation in light transmittance [col. 14, line 47 – col. 15, line 17]. It would therefore have been obvious to one of ordinary skill

in the art at the time of the invention to overlap the pixel electrode and the black matrix, motivated by the example and teaching of *Murade*. Claim 34 is therefore unpatentable.

Allowable Subject Matter

11. Claim 41 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

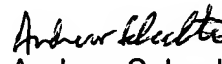
The prior art does not disclose the method of claim 41, in particular the additional limitations of patterning the conductive layer to simultaneously form the gate line and the buffer layer, wherein the gate line and the buffer layer are electrically disconnected. (Prior art such as U.S. Patent No. 6,067,131 to *Sato* does disclose buffer layers which are electrically disconnected from the gate line, but not also having the gate line and buffer layer simultaneously formed.) Claim 41 would therefore be allowable if rewritten appropriately.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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13 March 2005